

- 1 1. A method for forming a semiconductor structure, the method comprising:
2 providing a substrate;
3 forming a semiconductor layer over a top surface of the substrate, the
4 semiconductor layer including at least two elements, the elements being distributed to
5 define an initial compositional variation within the semiconductor layer; and
6 annealing the semiconductor layer to reduce the initial compositional variation.
- 1 2. The method of claim 1 wherein the substrate has a first lattice constant, the
2 semiconductor layer has a second lattice constant, and the first lattice constant differs
3 from the second lattice constant.
- 1 3. The method of claim 1 wherein a first element has a first concentration, a second
2 element has a second concentration, and each of the first and second concentrations is at
3 least 5%.
- 1 4. The method of claim 1 wherein the initial compositional variation varies
2 periodically within the semiconductor layer in a direction perpendicular to a
3 semiconductor layer deposition direction.
- 1 5. The method of claim 4 wherein the compositional variation defines a column
2 within the semiconductor layer, the column having a width and a period.
- 1 6. The method of claim 5 wherein the columnar period is less than approximately
2 2000 nanometers.
- 1 7. The method of claim 6 wherein the columnar period is less than approximately
2 1000 nanometers.
- 1 8. The method of claim 5 wherein the semiconductor layer is annealed at an
2 annealing temperature sufficient to diffuse at least one of the two elements through a
3 diffusion length at least equal to a quarter of the columnar period.

- 1 9. The method of claim 5 wherein the semiconductor layer is annealed for a duration
2 sufficient to diffuse at least one of the two elements through a diffusion length at least
3 equal to a quarter of the columnar period.
- 1 10. The method of claim 1 wherein the initial compositional variation varies in a
2 direction parallel to a semiconductor layer deposition direction and defines a superlattice
3 having a periodicity.
- 1 11. The method of claim 10 wherein the superlattice periodicity is less than
2 approximately 100 nanometers.
- 1 12. The method of claim 11 wherein the superlattice periodicity is less than
2 approximately 50 nanometers.
- 1 13. The method of claim 12 wherein the superlattice periodicity is less than
2 approximately 10 nanometers.
- 1 14. The method of claim 10 wherein the semiconductor layer is annealed at an
2 annealing temperature sufficient to diffuse at least one of the two elements through a
3 diffusion length at least equal to a quarter-period of the superlattice.
- 1 15. The method of claim 10 wherein the semiconductor layer is annealed for a
2 duration sufficient to diffuse at least one of the two elements through a diffusion length at
3 least equal to a quarter-period of the superlattice.
- 1 16. The method of claim 1 wherein the semiconductor layer is annealed at an
2 annealing temperature greater than the deposition temperature.
- 1 17. The method of claim 16 wherein the annealing temperature is greater than about
2 800 °C.
- 1 18. The method of claim 17 wherein the annealing temperature is greater than about
2 1000 °C.

- 1 19. The method of claim 1 wherein the semiconductor layer is annealed at an
2 annealing temperature below a melting point of the semiconductor layer.
- 1 20. The method of claim 19 wherein the annealing temperature is less than about
2 1270°C.
- 1 21. The method of claim 1 wherein one of the at least two elements comprises silicon.
- 1 22. The method of claim 1 wherein one of the at least two elements comprises
2 germanium.
- 1 23. The method of claim 1, further comprising:
2 planarizing a top surface of the semiconductor layer.
- 1 24. The method of claim 23 wherein the top surface of the semiconductor layer is
2 planarized before the semiconductor layer is annealed.
- 1 25. The method of claim 23 wherein the top surface of the semiconductor layer is
2 planarized while the semiconductor layer is annealed.
- 1 26. The method of claim 22 wherein the top surface of the semiconductor layer is
2 planarized after the semiconductor layer is annealed.
- 1 27. The method of claim 22 wherein planarizing comprises at least one of chemical-
2 mechanical polishing, plasma planarization, wet chemical etching, gas-phase chemical
3 etching, oxidation followed by stripping, and cluster ion beam planarization.
- 1 28. The method of claim 27 wherein chemical-mechanical polishing comprises a first
2 and a second step and the semiconductor layer is annealed between the first and the
3 second chemical-mechanical polishing steps.
- 1 29. The method of claim 27 wherein chemical-mechanical polishing comprises a first
2 and a second step and the semiconductor layer is annealed before the first chemical-
3 mechanical polishing step.

- 1 30. The method of claim 27 wherein planarization comprises a high temperature step
2 and the semiconductor layer is annealed during the high temperature planarization step.
- 1 31. The method of claim 23, further comprising:
2 bonding a top surface of the semiconductor layer to a wafer; and
3 removing at least a portion of the substrate,
4 wherein at least a portion of the semiconductor layer remains bonded to the wafer
5 after the portion of the substrate is removed.
- 1 32. The method of claim 23, further comprising:
2 forming a second layer over the semiconductor layer subsequent to planarizing
3 the top surface of the semiconductor layer.
- 1 33. The method of claim 32 wherein the second layer comprises a material having a
2 lattice constant substantially equal to a lattice constant of the semiconductor layer.
- 1 34. The method of claim 32 wherein the second layer comprises a material having a
2 lattice constant substantially different from a lattice constant of the semiconductor layer.
- 1 35. The method of claim 32, further comprising:
2 bonding a top surface of the second layer to a wafer; and
3 removing at least a portion of the substrate,
4 wherein at least a portion of the second layer remains bonded to the wafer after
5 the portion of the substrate is removed.
- 1 36. The method of claim 32 wherein the second layer comprises (i) a lower portion
2 having a superlattice and (ii) an upper portion disposed over the lower portion, the upper
3 portion being substantially free of a superlattice.
- 1 37. The method of claim 1 wherein the semiconductor layer has an undulating
2 surface.
- 1 38. The method of claim 33 wherein the undulating surface is formed during
2 deposition of the semiconductor layer.

- 1 39. The method of claim 38 wherein the substrate has an undulating substrate surface
2 and the undulating substrate surface induces the formation of the undulating surface of
3 the semiconductor layer.
- 1 40. The method of claim 37 wherein the undulating surface has an amplitude, the
2 initial compositional variation defines a superlattice having a periodicity, and the
3 periodicity of the superlattice is less than the amplitude of the undulating surface.
- 1 41. The method of claim 1, further comprising:
2 forming a relaxed graded layer over the substrate,
3 wherein the semiconductor layer is formed over the relaxed graded layer.
- 1 42. The method of claim 1, further comprising:
2 forming a protective layer over the semiconductor layer prior to annealing the
3 semiconductor layer.
- 1 43. The method of claim 42 wherein the protective layer comprises a material that is
2 substantially inert with respect to the semiconductor layer.
- 1 44. The method of claim 43 wherein the protective layer is selected from the group
2 consisting of silicon dioxide, silicon nitride, and combinations thereof.
- 1 45. A method for forming a semiconductor structure, the method comprising:
2 providing a substrate;
3 selecting a first plurality of parameters suitable for forming a semiconductor layer
4 over a top surface of the substrate, the semiconductor layer including at least two
5 elements, the elements being distributed to define a compositional variation within the
6 semiconductor layer;
7 forming the semiconductor layer having a haze; and
8 planarizing the semiconductor layer to remove the haze.
- 1 46. The method of claim 45 wherein forming the semiconductor layer comprises
2 forming a lower portion including a superlattice and forming an upper portion over the
3 lower portion, the upper portion being substantially free of a superlattice.

- 1 47. The method of claim 45 wherein the first plurality of parameters comprises at
2 least one parameter selected from the group consisting of temperature, precursor, growth
3 rate, and pressure.
- 1 48. The method of claim 45, further comprising:
2 cleaning the semiconductor layer after planarizing,
3 wherein the semiconductor layer remains substantially haze-free after cleaning.
- 1 49. The method of claim 45, further comprising:
2 selecting a second plurality of parameters suitable for forming a substantially
3 haze-free regrowth layer over the semiconductor layer, the semiconductor layer including
4 at least two elements, the elements being distributed to define a compositional variation
5 within the semiconductor layer; and
6 forming the substantially haze-free regrowth layer.
- 1 50. The method of claim 49 wherein the first plurality of parameters comprises a first
2 temperature, the second plurality of parameters comprises a second temperature, and the
3 first temperature is higher than the second temperature.
- 1 51. The method of claim 49 wherein the first plurality of parameters comprises a first
2 growth rate, the second plurality of parameters comprises a second growth rate, and the
3 first growth rate is higher than the second growth rate.
- 1 52. The method of claim 49 wherein forming the regrowth layer comprises forming a
2 lower portion including a superlattice and forming an upper portion over the lower
3 portion, the upper portion being substantially free of a superlattice.
- 1 53. A semiconductor structure comprising:
2 a substrate; and
3 a semiconductor layer disposed over the substrate, the semiconductor layer
4 including at least two elements and having a top surface,
5 wherein the semiconductor layer top surface is substantially haze-free.

- 1 54. The structure of claim 53 wherein a portion of the semiconductor layer disposed
2 below the top surface comprises a superlattice.
- 1 55. The structure of claim 53, further comprising:
2 a relaxed graded layer disposed between the substrate and the semiconductor
3 layer.
- 1 56. The structure of claim 53 wherein the semiconductor layer top surface has a
2 roughness root-mean-square of less than 5 angstroms in a scan area of $40\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$,
3 and a contamination level of less than $0.29\text{ particles/cm}^2$, the particles having a diameter
4 greater than 0.12 micrometers.
- 1 57. The structure of claim 56 wherein the roughness is less than 1 angstrom root-
2 mean-square in a scan area of $1\text{ }\mu\text{m} \times 1\text{ }\mu\text{m}$.
- 1 58. The structure of claim 53 wherein the semiconductor layer top surface has a
2 roughness of less than 5 angstroms root-mean-square in a scan area of $40\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$
3 and a contamination level of less than $0.16\text{ particles/cm}^2$, the particles having a diameter
4 greater than 0.16 micrometers.
- 1 59. The structure of claim 58 wherein the roughness is less than 1 angstrom root-
2 mean-square in a scan area of $1\text{ }\mu\text{m} \times 1\text{ }\mu\text{m}$.
- 1 60. The structure of claim 53 wherein the semiconductor top surface has a roughness
2 of less than 5 angstroms root-mean-square in a scan area of $40\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$ and a
3 contamination level of less than $0.08\text{ particles/cm}^2$, the particles having a diameter greater
4 than 0.2 micrometers.
- 1 61. The structure of claim 60 wherein the roughness is less than 1 angstrom root-
2 mean-square in a scan area of $1\text{ }\mu\text{m} \times 1\text{ }\mu\text{m}$.
- 1 62. The structure of claim 53 wherein the semiconductor layer top surface has a
2 roughness of less than 5 angstroms root-mean-square in a scan area of $40\text{ }\mu\text{m} \times 40\text{ }\mu\text{m}$
3 and a contamination level of less than $0.019\text{ particles/cm}^2$, the particles having a diameter
4 greater than 1 micrometer.

- 1 63. The structure of claim 62 wherein the roughness is less than 1 angstrom root-
2 mean-square in a scan area of $1\ \mu\text{m} \times 1\ \mu\text{m}$.
- 1 64. The structure of claim 53 wherein the semiconductor layer top surface has a
2 roughness of less than 0.5 angstroms root-mean-square in a scan area of $1\ \mu\text{m} \times 1\ \mu\text{m}$ and
3 a contamination level of less than 0.09 particles/cm², the particles having a diameter
4 greater than 0.09 micrometers.
- 1 65. A semiconductor structure comprising:
2 a substrate;
3 a semiconductor layer disposed over the substrate, the semiconductor layer
4 including at least two elements; and
5 a regrowth layer disposed over the semiconductor layer, the regrowth layer having
6 a top surface,
7 wherein the regrowth layer top surface is substantially haze-free.
- 1 66. The structure of claim 65 wherein the regrowth layer comprises a semiconductor
2 material.
- 1 67. The structure of claim 66 wherein the regrowth layer comprises silicon.
- 1 68. The structure of claim 65 wherein the regrowth layer is strained.
- 1 69. The structure of claim 65 wherein a portion of the regrowth layer disposed below
2 the regrowth layer top surface comprises a superlattice.
- 1 70. A semiconductor structure comprising:
2 a wafer, and
3 a semiconductor layer bonded to the wafer, the semiconductor layer having a top
4 surface,
5 wherein the semiconductor layer top surface is substantially haze-free.
- 1 71. The structure of claim 70 wherein the semiconductor layer comprises silicon.
- 1 72. The structure of claim 70 wherein the semiconductor layer is strained.

- 1 73. The structure of claim 70 wherein the semiconductor layer comprises germanium.
- 1 74. The structure of claim 70 wherein the wafer comprises an insulating layer.
- 1 75. The structure of claim 74 wherein the insulating layer comprises silicon dioxide.